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Formation of self-aligned $CoSi_2$ on selective epitaxial growth silicon layer on (001)Si inside 0.1–0.6 μm oxide openings prepared by electron beam lithography

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The self-aligned formation of $CoSi_2$ was achieved on the selective epitaxial growth (SEG) silicon layer on (001)Si inside 0.1–0.6 μm oxide openings prepared by electron beam lithography. The uniform, high quality SEG Si layer was grown by ultrahigh vacuum chemical vapor deposition at 560 °C with Si_2H_6. Self-aligned $CoSi_2$ film without lateral growth of silicide was grown on the SEG Si layer by rapid thermal annealing at 700 °C in N_2 ambient. The successful integration of the self-aligned $CoSi_2$ and SEG of Si processes promises to be a viable process technology for the future deep submicron devices. © *1996 American Institute of Physics.* [S0003-6951(96)02450-3]

As the microelectronics device dimensions scale down to the deep submicron level, silicides in the source/drain area are needed to reduce the contact resistance to an acceptable level. The self-aligned silicide (SALICIDE) process has been generally used for gate, source, and drain metallization in microelectronics devices. Although low-resistivity $TiSi_2$ is currently the most common silicide for this application, $CoSi_2$ is the only silicide that offers properties and reliability for continued use in the sub-0.25 μm devices.[1] However, the consumption ratio of the substrate silicon to Co to form $CoSi_2$ is as high as 3.6 in the direct interaction of Co with the substrate silicon. The high consumption ratio is a critical drawback for the formation of self-aligned $CoSi_2$ on shallow junctions since it results in the series resistance increase and degradation of junction integrity.[2]

Elevated source/drain structures are a potential solution to many of the problems by the deposition of an ultrashallow and defect-free junction.[3–5] The common approach to fabricating elevated source and drain has been the selective epitaxial growth of silicon (SEG-Si) on the source and drain areas. Selective epitaxial growth is a method in which an epitaxial layer can be grown on the exposed silicon without growing polycrystalline silicon on the SiO_2.[6–8] To achieve low-temperature SEG-Si, a promising technique is ultrahigh vacuum chemical vapor deposition (UHV-CVD). High quality epitaxial silicon layer has been grown on exposed Si by applying UHV-CVD with disilane (Si_2H_6) as the source on silicon wafers with oxide patterns.[9–12]

In this letter, we report the successful integration of the self-aligned $CoSi_2$ and SEG-Si processes inside 0.1–0.6 μm oxide openings prepared by electron beam lithography. The scheme promises to be a viable process technology for the future deep submicron devices.

The patterned oxide wafers were prepared by using the electron beam lithography (EBL) and reactive ion etching (RIE). Six-in. diam, boron doped (001) Si wafers, 1–20 ohm cm in resistivity, were first cleaned by standard RCA process followed by a low pressure chemical vapor deposition (LPCVD) to form a 160-nm-thick silicon dioxide at 700 °C in decomposing tetraethoxysilane (TEOS), $Si(OC_2H_5)_4$. The electron beam exposure system utilized was of the model EBML300 made by Leica Cambridge. The etching process is composed of two steps, oxide etching and *in situ* post etching treatment using CF_4CHF_3/Ar and CF_4/O_2 gas mixtures, respectively. The oxide opening patterns consist of 0.1–0.6 μm linear openings and contact holes.

Prior to loading into the UHV-CVD chamber, the wafers were chemically cleaned in H_2SO_4/H_2O_2 and $NH_4OH/H_2O_2/H_2O$ and dipped in a dilute HF solution ($HF:H_2O=1:200$). The base pressure of the UHV-CVD system was 2×10^{-10} Torr after 6 h of baking. Prior to the SEG-Si, the native oxide on the Si surface was removed by a thermal process. The *in situ* thermal cleaning process was done at 860 °C for 5 min. The SEG-Si temperature was 560 °C and the deposition time was 30 min. The Si_2H_6 gas flow rate was 0.5 sccm.

After the SEG-Si, the wafers were dipped in the dilute HF solution before loading into an electron gun evaporation system. The 30-nm-thick Co thin films were then electron beam deposited onto the patterned substrates. The vacuum during the deposition was maintained to be better than 1

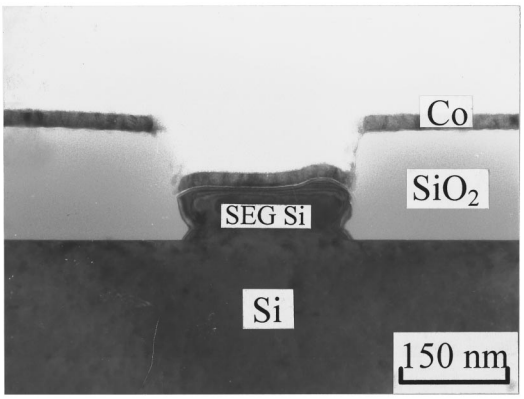

FIG. 1. Cross-section TEM image (taken along the [110] direction) of the as-deposited Co film on SEG Si layer inside 0.2 μm linear oxide opening.

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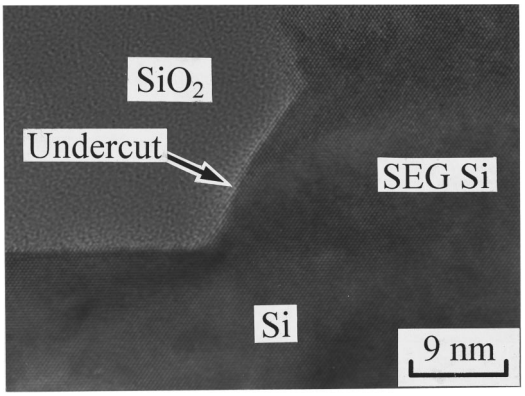

FIG. 2. HRTEM image of the interfaces between SEG Si and Si substrate as well as the oxide sidewall.

$\times 10^{-6}$ Torr. The deposition rate was 0.05 nm/s. The silicidation reaction was carried out in a rapid thermal annealing system in N_2 ambient. The samples were annealed at 400–900 °C with a heating rate of 100 °C/s and annealing time of 60 s. Selective nonreacted Co removal was carried out in an etchant solution ($HCl:H_2O_2=3:1$). The surface morphology of the oxide openings was observed by a Hitachi S-4000 field emission scanning electron microscope. A JEOL 200CX scanning transmission electron microscope (TEM) operating at 200 kV was used for obtaining microstructural information. For high resolution TEM observation, a JEOL 4000EX operating at 400 kV with a point-to-point resolution of 0.18 nm was used.

Figure 1 shows a cross-section TEM (XTEM) image (taken along the [110]Si direction) of the as-deposited Co film on SEG Si layer inside a 0.2 μm linear opening. Conformal coverage of the deposited Co film on the SEG Si layer inside the oxide opening is evident. The interface between the epitaxial silicon and silicon substrate is discrete and sharp. The success of the SEG-Si demonstrates that the *ex situ* wet cleaning and *in situ* thermal cleaning processes were effective in removing the native oxide on the exposed silicon inside oxide openings.

The surface morphology of the SEG Si film appears to be uneven due to nonuniform etching of the oxide pattern and undercutting of oxide wall. The epitaxial silicon was grown on the exposed silicon inside a 0.2 μm linear opening. No polycrystalline silicon was found to grown on the SiO_2. The epitaxial growth is therefore considered to be surface reaction limited, which is expected at the growth temperature of 560 °C. The thickness of the SEG Si film is 80 nm and is independent of the size of oxide openings. The epitaxial growth rate was measured to be 2.7 nm/min. A HRTEM image of the interfaces of SEG Si/Si substrate and SEG Si/sidewall oxide is shown in Fig. 2. The epitaxial silicon is seen to be of rather high quality. No extended defects such as stacking faults or dislocations were observed to be present. It is worthwhile to note that oxide undercutting is an important issue in the SEG-Si process. Typically, oxide undercutting occurs during the thermal cleaning step prior to the SEG-Si deposition.[13,14]

Figure 3(a) shows a cross-section SEM image of a 0.18 μm contact hole. Good anisotropy is seen in the profile of the oxide opening although the sidewall is somewhat rugged due to the nonuniform etching of the oxide wall. Figure 3(b) shows the as-deposited Co film on the SEG Si layer inside a 0.13 μm contact hole. Figure 3(c) shows a SEM image of $CoSi_2$ formed on the SEG Si layer inside a 0.2 μm contact

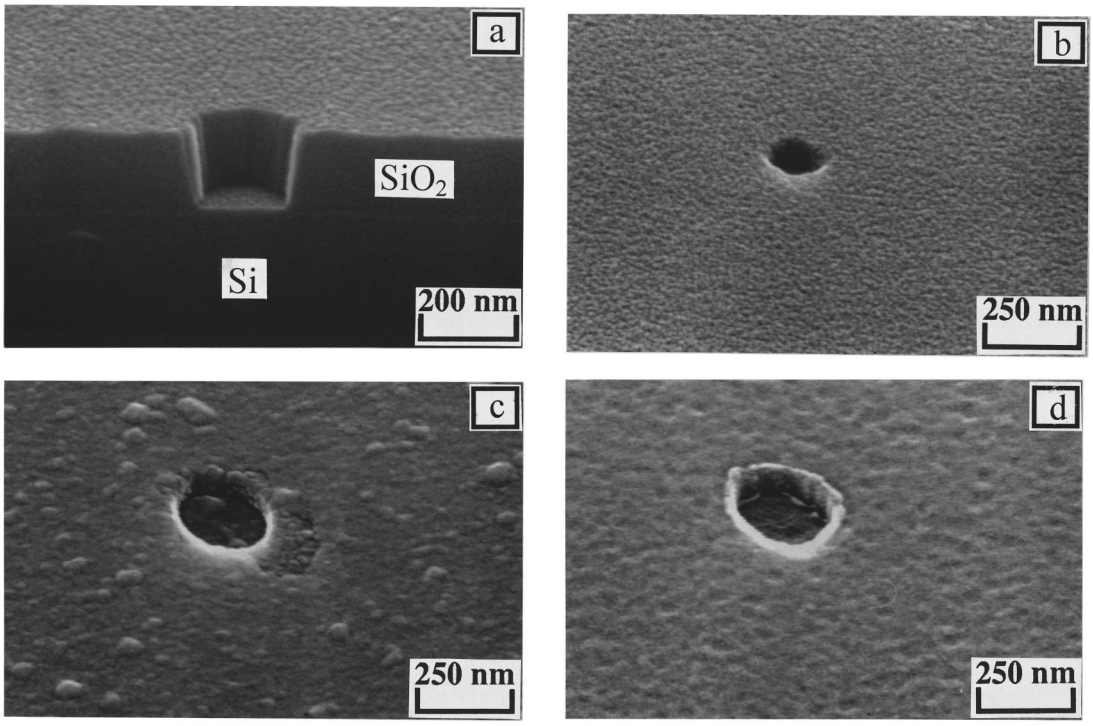

FIG. 3. SEM images of (a) a 0.18 μm contact hole, cross-section, (b) as-deposited Co film on the SEG Si layer inside a 0.13 μm contact hole, (c) $CoSi_2$ formed on the SEG Si layer inside a 0.2 μm contact hole after RTA treatment at 700 °C, (d) selectively etched $CoSi_2$ film on the SEG Si layer inside a 0.23 μm contact hole after RTA treatment at 700 °C.

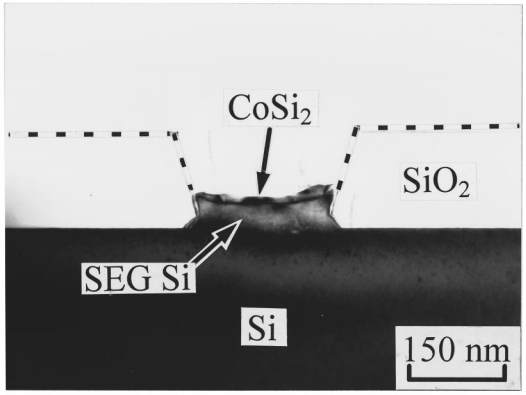

FIG. 4. Cross-section TEM image of the $CoSi_2$ film on the SEG Si layer inside a 0.23 μm linear opening after RTA at 700 °C and selective etching treatment.

hole after RTA treatment at 700 °C. It reveals that the Co starts to ball up on the SiO_2 layer. Figure 3(d) shows a SEM image of selectively etched $CoSi_2$ film on the selective epitaxial layer inside a 0.23 μm contact hole after RTA treatment at 700 °C. The nonreacted metal was removed successfully and a smooth top layer of silicide on the SEG Si layer was formed.

Cross-section TEM image of the $CoSi_2$ film on the SEG Si layer inside a 0.23 μm contact hole after RTA treatment at 700 °C is shown in Fig. 4. The 15-nm-thick $CoSi_2$ was formed on the SEG Si layer without lateral growth of the silicide. The absence of lateral silicide overgrowth has been reported.[15] It was suggested to be related to the physical disconnection between the Co globules and the $CoSi_2$ layer, preventing any further reaction.

A low density of small oxygen clusters were revealed by the TEM to be present at the SEG Si/Si substrate interface. The oxygen clusters are smaller in size compared to those of oxide openings. Oxygen clusters were previously observed to form at the SEG Si/Si substrate interface.[16] The formation of the oxygen clusters is expected to impede the epitaxial growth of silicon above the clusters. However, at the growth temperature, the silicon lattice around the clusters overgrows and coalesces at the top of the small and discrete clusters.

In the future deep subquarter micron metal-oxide-semiconductor field effect transistor device structure, the separation distance of silicide region is often less than quarter micrometer in some areas. A good self-alignment without lateral overgrowth is required in the SALICIDE process. Although the SEG is common for advanced devices, the report on the successful implementation of SEG-Si at low temperature by UHV-CVD inside deep submicron devices is relatively recent and rare.[12] In addition, the growth of $CoSi_2$ layer, which is considered to be the most promising contact material for the sub-0.25 micron devices, on SEG-Si inside deep submicron oxide openings was never achieved before. Both $CoSi_2$ and SEG-Si are part of the scheme for the fabrication of deep subquarter micron devices. The successful integration of the self-aligned $CoSi_2$ and SEG-Si processes promises to be a viable process technology for the future devices.

In summary, the SEG Si was grown by UHV-CVD on (001)Si inside 0.1–0.6 μm oxide openings. The SEG Si is of high quality without the formation of growth defects as observed by HRTEM. The thickness of the epitaxial selective silicon film is independent of the size of oxide openings. The formation of self-aligned $CoSi_2$ without lateral growth of silicide on the SEG Si layer inside 0.1–0.6 μm oxide openings was achieved by rapid thermal annealing at 700 °C in N_2 ambient.

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