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Thin Silicon Dioxide Using the Rapid Thermal Oxidation (RTO) Process for Trench Capacitors

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ABSTRACT

Growth and electrical characteristics of thin silicon dioxide using the rapid thermal oxidation (RTO) process have been studied for planar and trench capacitors. Growth of silicon dioxide follows the linear-parabolic model. The activation energies of the linear rate constant B/A and the parabolic rate constant B are found to be 1.98 and 1.42 eV, respectively. Good electrical characteristics can be achieved by increasing the oxidation temperature from 1000° to 1150°C. For the trench capacitors oxidized at 1150°C, it is found that oxide breakdown occurs dominantly at the fields 10 ~ 12 mV/cm, the leakage current density is 3×10^{-11} A/cm^2 and the interface-state density is 3×10^{10} cm^{-2} eV^{-1}. The RTO process is proved to be a promising technique for the fabrication of trench capacitors.

For DRAM (dynamic random access memory) devices, increasing the packing density has been strongly required. To increase packing density, while keeping the capacitance large enough to prevent radiation-induced soft errors, reducing the occupation area of capacitors is essential. For the DRAM below 1 Mbit, planar capacitors have been used. The decrease in capacitance due to the area reduction has been compensated for by the increase in capacitance due to the reduction in thickness of the silicon dioxide film. For the DRAM above 1 Mbit trench capacitors are required to get high packing density instead of the planar capacitors. Growth of the high quality and reliable silicon dioxide film can be performed at high temperature (>1000°C) by controlling the short oxidation time precisely. This condition is required especially in the formation of the high quality and reliable thin silicon dioxide film for the trench capacitors. The trench capacitors have right-angled corners at the top and the bottom of the trench. The stress concentration causes oxide thinning at corners (1, 2). The dielectric breakdown voltage of the trench capacitors is limited by that at the corners and is lower than that of the planar capacitors. This problem can be solved by the stress relief due to viscous flow of silicon dioxide at high temperature (3). Using conventional furnace at the high temperature, it is difficult to control precisely the growth of thin thermal oxide film without impurity redistribution. On the other hand, rapid thermal oxidation (RTO) process (4-7) has been investigated recently, because the rapid thermal heating system is proper for the operation at high temperatures and short times and for the growth of the high quality and reliable thin gate oxide film. We have adapted the RTO process for the fabrication of trench capacitors.

The studies of the planar and the trench capacitors fabricated using RTO process are reported. Sample fabrication of the planar and the trench capacitors and measurements are described in the Experiment section. Growth of silicon dioxide and electrical characteristics of the planar capacitors are reported in the Results and Discussion section. Electrical characteristics of the trench capacitors are described in section on the Results and Discussion section.

Experiment

Sample fabrication.—The fabrication flow of MOS capacitors is shown in Fig. 1. The CZ silicon wafers are of 150 mm diam, 650 μm thickness, (100) orientation, and 10 ~ 15 Ωcm resistivity (boron-doped). After cleaning chemically the surface of wafer, the 50 nm thickness oxide layer was formed with conventional furnace. Silicon nitride of 120 nm thickness was deposited by LPCVD. B^+ ions were implanted to form the channel-stop region. LOCOS of 700 nm thickness was formed for isolation. The 50 nm thick silicon dioxide and 120 nm thick silicon nitride layers were etched chemically.

In the case of the trench capacitors, the 1000 nm thick silicon dioxide layer was deposited by CVD. The optical lithography step was done to produce the patterns on the silicon dioxide layer. The silicon dioxide layer was etched by reactive ion etching (RIE) with a photoresist mask. The silicon trenches were fabricated by RIE technique using the silicon dioxide film as etching mask. The trenches formed have 1×3 μm^2 area and 4 μm depth. The RIE system is equipped with a racetrack-type magnetron discharge (8). A mixture of $SiCl_4$, Cl_2, and SF_6 was used as the etching gas.

Gate oxide was grown by using the RTO process. The RTO apparatus (ULVAC LCA-1201) is shown in Fig. 2.

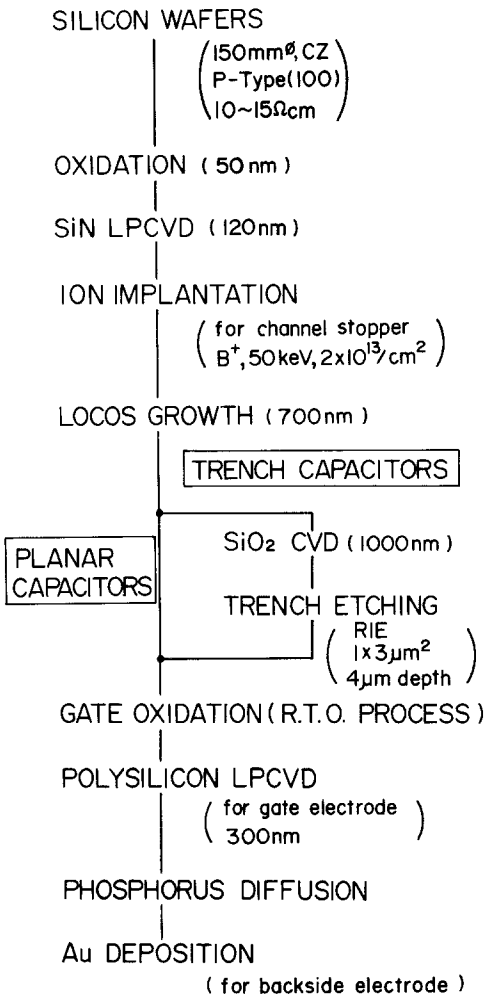

Fig. 1. Fabrication flow of MOS capacitors

After reducing the pressure to 10 Pa, O_2 gas was introduced into the chamber. The wafer was heated by tungsten-halogen lamps which had the heating rate of about 70°C/s and steady-state temperatures (oxidation temperatures) of 1000°, 1030°, 1100°, and 1150°C. This temperature-time profile is shown in Fig. 3. The 300 nm thick polysilicon layer of gate electrode was deposited on the gate oxide layer by LPCVD at 610°C and doped by $POCl_3$ diffusion at 950°C for 15 min. Au was deposited on the back side as an electrode. Figures 4 and 5a show the cross sections of the planar capacitors and of the trench capacitors, respectively. Figure 5b shows the SEM photograph of the trench capacitors.

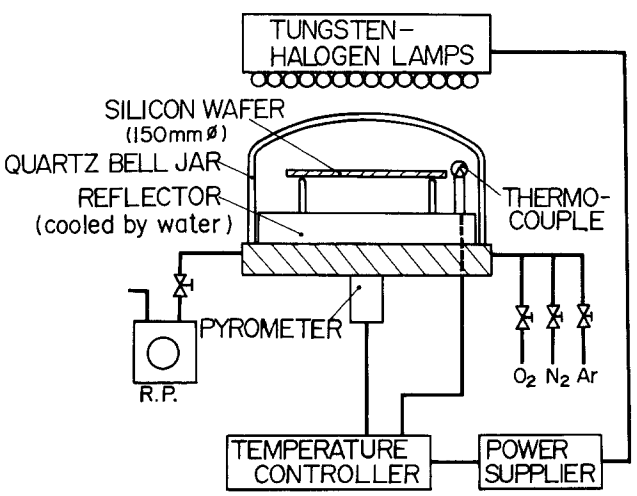

Fig. 2. RTO apparatus

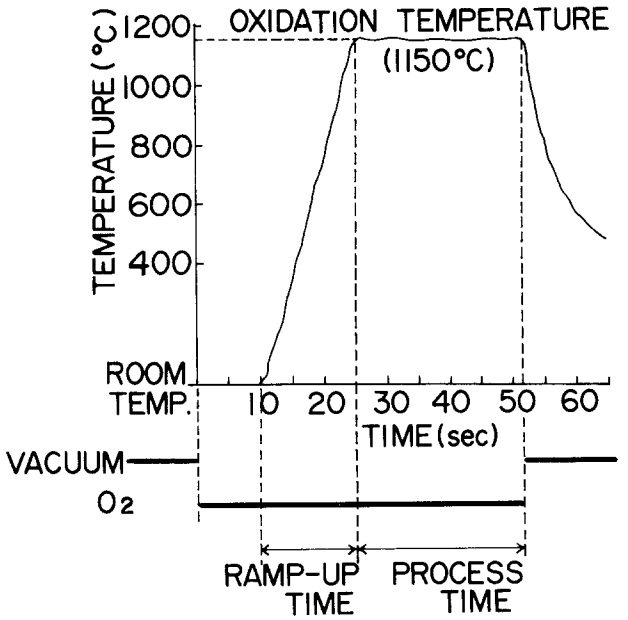

Fig. 3. Temperature-time profile of RTO process

Measurements.—The thickness of the silicon dioxide film was measured by means of a Gaertner Model L115B ellipsometer using 632.8 nm incident light. The refractive indexes of silicon and silicon dioxide were 3.85-i0.02 and 1.460, respectively, at a wavelength of 632.8 nm.

The dielectric breakdown measurements were made on the samples with oxide of 10 nm thickness and of 10 mm^2 gate area for the planar capacitors and with oxide of 14 nm thickness and of 25.6 mm^2 gate area for the trench capacitors. For the trench capacitors the oxide thickness was measured on the plane part of the trench capacitors (which consist of trench part and plane part).

The dielectric breakdown electric field was derived from the voltage at the current density 10^{-4} A/cm^2. Negative voltage was applied to the gate electrode. Then, silicon surface was the accumulation region, and the entire electric field was applied across the oxides. For the planar and trench capacitors 272 samples were used at each oxidation temperature.

For the current-voltage characteristics, the current was measured by applying negative voltage to the gate electrode.

Interface-state density measurements were made by using the quasi-static C-V method with the applied voltage sweep rate dv/dt = 0.1 V/s (9).

For the transient response of capacitance, the capacitance was measured after changing the applied voltage from −5V (accumulation state) to +5V (deep depletion state) as a function of time (10).

The measurements of the time dependent dielectric breakdown (TDDB) (11) were made under constant current (0.05, 0.1, 0.2, 0.4 A/cm^2). Negative voltage was ap-

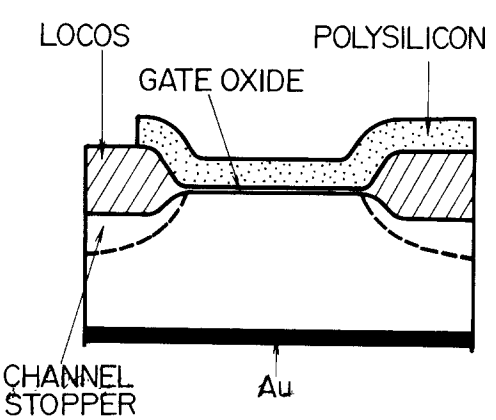

Fig. 4. Cross section of planar capacitors

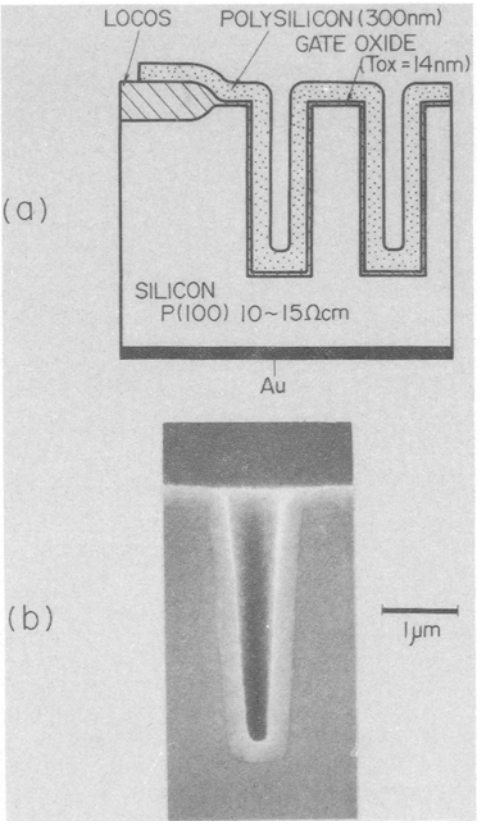

Fig. 5. (a) Cross section of trench capacitors. (b) SEM photograh of trench capacitors.

plied to the gate electrode. This breakdown is destructive and 136 samples were used at each measuring point.

Results and Discussion

Planar capacitors.—Growth of silicon dioxide.—Figure 6 shows the thickness of the silicon dioxide layer *vs.* oxidation time. These data are in good agreement with the quadratic curves shown by solid lines which are expected from the linear-parabolic model. This result indicates that kinetics of silicon dioxide growth using the RTO process follows the linear-parabolic model (12) in which the diffusion of the oxidant through silicon dioxide layer and the chemical reaction between Si and O_2 at the silicon-silicon dioxide interface are the limiting processes.

From Fig. 6 the parabolic rate constant B and linear rate constant B/A were derived for each oxidation tem-

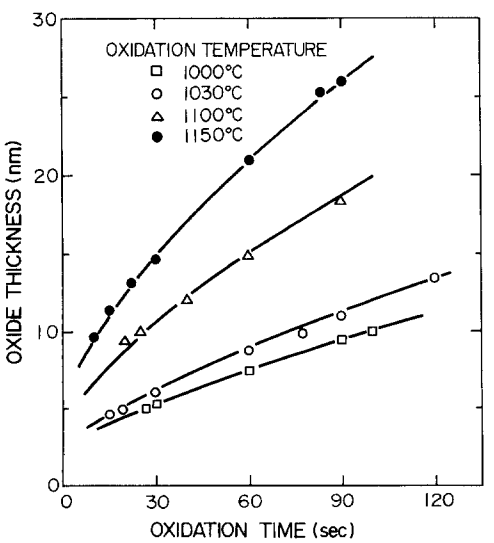

Fig. 6. Oxide thickness *vs.* oxidation time

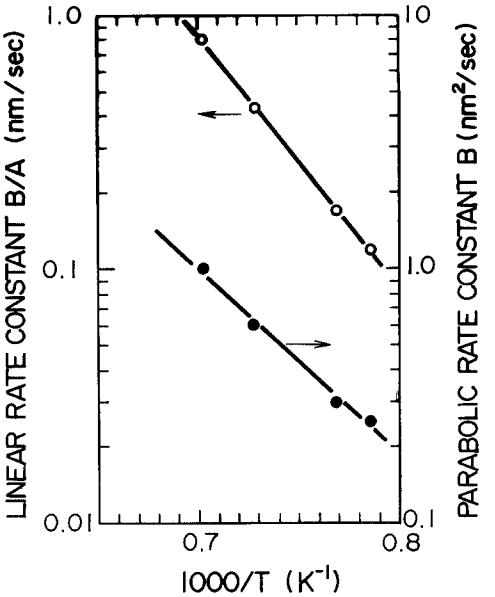

Fig. 7. Temperature dependence of linear rate constants (*B/A*) and parabolic rate constants (*B*).

perature. These values are shown in Fig. 7. The activation energies E_a of linear rate constant and of parabolic rate constant are estimated to be 1.98 and 1.42 eV, respectively. These activation energy values are reasonably similar to those of the oxidation using the conventional furnace (12). On the other hand, the activation energies for RTO processing have been reported in several papers (4-7) and are different from one another. The reason for these differences are not known.

Dielectric breakdown.—Dielectric breakdown frequency *vs.* breakdown fields is shown in the histograms in Fig. 8. Most of the dielectric breakdown occurs at high fields (>10 MV/cm) due to intrinsic dielectric strength (13) for every oxidation temperature 1000°, 1100°, and 1150°C. For both 1100° and 1150°C oxidation temperatures, low field breakdowns (<1 MV/cm) due to pinholes do not occur and medium field breakdowns (3 ~ 8 MV/cm) due to weak spots occur by a few percent.

Current-voltage characteristics.—Figure 9 shows current-voltage characteristics. The leakage current for

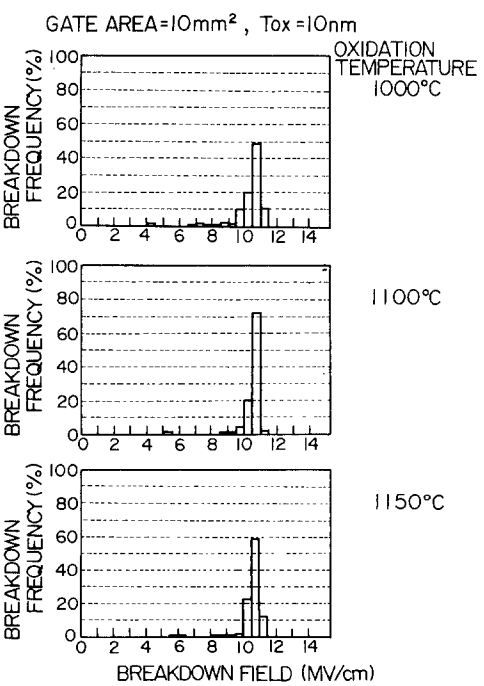

Fig. 8. Oxide breakdown field histogram for planar capacitors

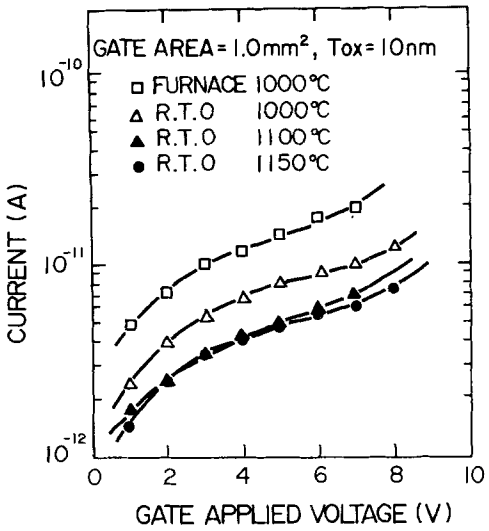

Fig. 9. Current-voltage characteristics

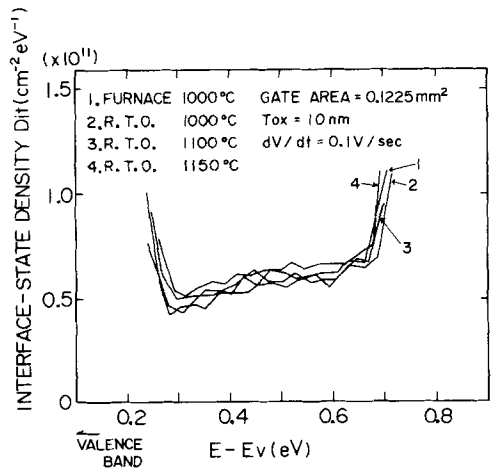

Fig. 10. Interface-state density as a function of energy in silicon bandgap.

RTO is below 10^{-11}A and smaller than that (shown as FURNACE 1000°C in Fig. 9) for the conventional furnace. The leakage current at 1100° and 1150°C oxidation temperatures is less than that at 1000°C oxidation temperature.

Interface-state density distribution.—Interface-state density distribution in the silicon bandgap is shown in Fig. 10. Interface-state density distribution is nearly independent of the oxidation temperature, and it has a U-shape in which the interface-state density is constant, and the value is 5×10^{10} cm^{-2} eV^{-1} in the midgap region 0.3-0.7 eV. These results show that rapid heating and cooling do not have a bad effect on the interface-state density.

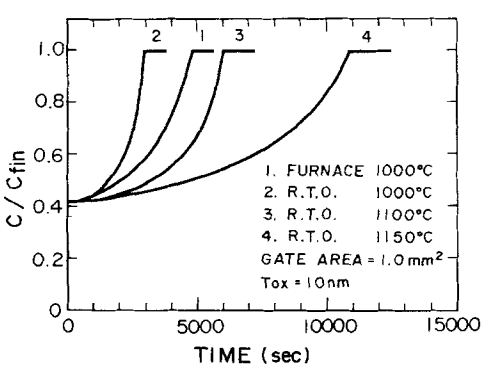

Fig. 11. Transient response of capacitance

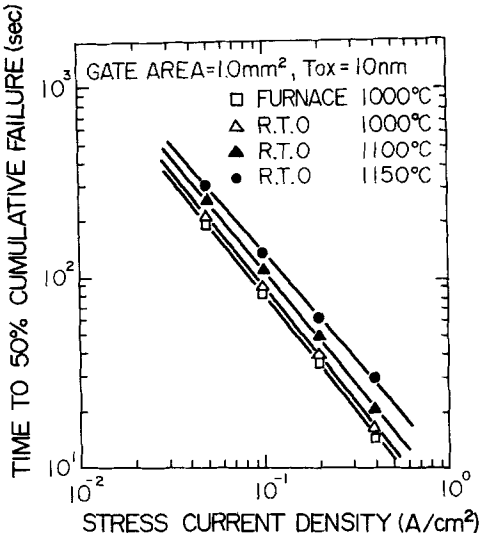

Fig. 12. Time to 50% cumulative failure as a function of stress current density.

Transient response of capacitance.—Figure 11 shows transient response of capacitance. As time progresses, the capacitance increases because the depletion layer width contracts due to generation of minority carriers, and returns to the final capacitance C_{fin} which is equal to the capacitance in the accumulation state. The time which is required for returning to C_{fin} increases with oxidation temperature; it is very long at 1150°C.

These results demonstrate that damage to the silicon surface layer is not caused by rapid heating and cooling above 1100°C oxidation temperature.

Time dependent dielectric breakdown (TDDB).—The measurements of TDDB are useful in estimating the lifetime of the silicon dioxide layer. Figure 12 shows the time to 50% cumulative failure as a function of stress current density. The lifetime of the silicon dioxide layer increases with oxidation temperature. The lifetime of the silicon dioxide layer formed by RTO and conventional furnace at 1000°C is very similar to each other.

Trench capacitors.—Dielectric breakdown.—The oxide dielectric breakdown field histogram is shown in Fig. 13. The dielectric breakdown frequency increases in the me-

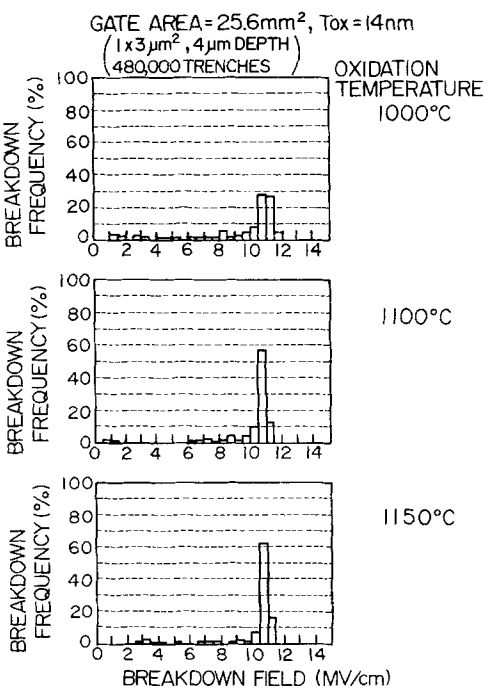

Fig. 13. Oxide breakdown fields histogram of trench capacitors

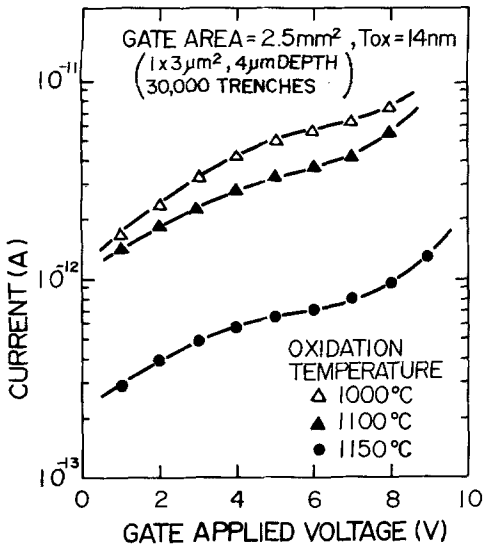

Fig. 14. Current-voltage characteristics of trench capacitors

dium field range for the trench capacitor compared with that for the planar capacitors.

Current-voltage characteristics.—Figure 14 shows current-voltage characteristics. Leakage current is very small at high oxidation temperature (1150°C). Leakage current of the trench capacitors is smaller than that of the planar capacitors because the silicon dioxide film of the trench capacitors is thicker than that of the planar capacitors.

Interface-state density distribution.—Figure 15 shows the interface-state density as a function of energy in the silicon bandgap. The interface-state density decreases with increasing oxidation temperature.

TDDB.—Time to 50% cumulative failure as a function of stress current density is shown in Fig. 16. The lifetime of the silicon dioxide layer increases with oxidation temperature, and it is shorter than that for the planar capacitors. The electrical acceleration factor in the time to breakdown measurement is 1.5 decades/MV/cm.

Good electrical characteristics were achieved by increasing the oxidation temperature from 1000° to 1150°C in the silicon dioxide layer, the interface between silicon and silicon dioxide and the silicon surface layer for the planar capacitors and the trench capacitors. We are sure

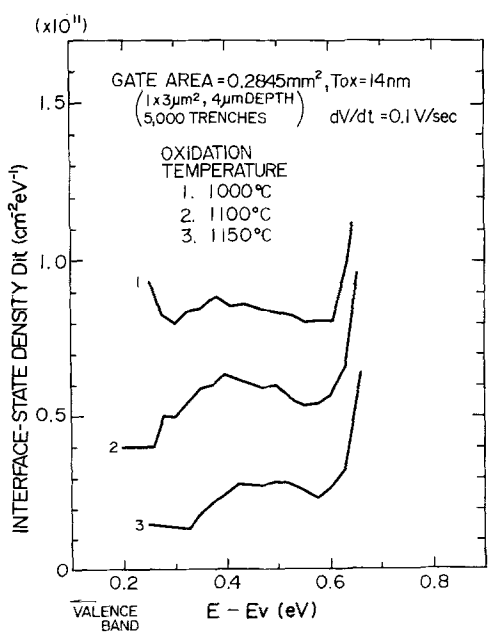

Fig. 15. Interface-state density as a function of energy in silicon bandgap (trench capacitors).

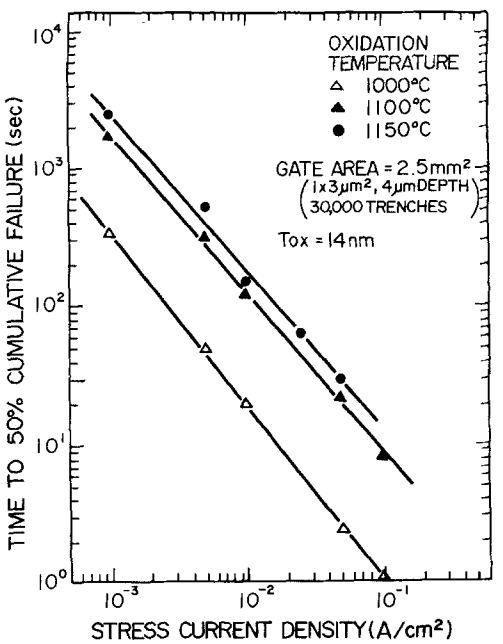

Fig. 16. Time to 50% cumulative failure as a function of stress current density (trench capacitors).

that these good results are achieved by the stress relief of the silicon dioxide due to the larger viscous flow of the silicon dioxide at higher temperature (>1000°C). (Of course, the dust and contamination-free process is required.)

Electrical characteristics of trench capacitors depend noticeably on the oxidation temperature compared with that of planar capacitors. This reason is that the trench capacitors have right-angled corners at which the stress concentrates strongly and the relaxation of the stress due to viscous flow of the silicon dioxide depends considerably on the oxidation temperature (3).

Conclusion

Plane capacitors and trench capacitors were fabricated using RTO process. Growth of silicon dioxide in the range 4 ~ 26 nm was investigated. It was found that the growth of silicon dioxide followed linear-parabolic model similar to the case using conventional furnace. Electrical characteristics are improved due to the stress relief of the silicon dioxide at high oxidation temperature. We suggest that the effect of the stress relief is important for the trench capacitors which have right-angled corners. The undesirable effect due to rapid heating and cooling is not found. The RTO process is superior to the process using the conventional furnace for the controllability of short oxidation time and high oxidation temperatures. The RTO process promises the useful process for the fabrication of the trench capacitors.

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Influence of Extended Defects and Native Impurities on the Electrical Properties of Directionally Solidified Polycrystalline Silicon

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ABSTRACT

The electrical properties of dislocations and grain boundaries (GB) in directionally solidified polycrystalline silicon were extensively studied as a function of the carbon, oxygen, and nitrogen content, as well as of the relative grain orientation. As a first result of this study we obtained the experimental evidence that the oxygen and carbon content are not independent variables of the material. Therefore, the density and the electrical activity of dislocations are shown to be strongly dependent on the amount of oxygen-carbon compensation. As a second result, experimental evidence was also achieved which demonstrated that grain boundaries are strongly passivated and that recombination losses at GB do not present any relevant relationship with mutual crystallographic orientations of the grains. It appears, therefore, that a careful choice of the growth and postgrowth conditions yields a material which behaves like crucible grown single-crystal silicon.

The possibility of achieving high efficiency solar cells with polycrystalline silicon is still a matter of hot discussion, as the role of the substrate with its microstructure, dislocation density, and native impurity content is not completely understood. This material's peculiarities depend essentially on the variety of growth and postgrowth conditions adopted by the manufacturers, so that polycrystalline silicon of different origins may show differences in this respect. In fact, at least the possibility exists that the configuration of structural defects, as well as the content and the distribution of native impurities between the volume and the GB in polycrystalline silicon, could be "lot dependent" or at least "manufacture dependent".

Attempts to apply to polycrystalline silicon a zero order model, which assumes homogeneous intragrain properties and constant GB recombination (1) has already failed, as a consequence of the intrinsic complexity of polycrystalline materials, where (*i*) interactions, often of chemical origin, between point defects and extended defects, dominate the electrical properties, (*ii*) intragrain defects, very often limit the diffusion length of minority carriers (1) and (*iii*) high temperature annealings enhance the electrical activity of recombination centers at GB (2, 3).

In single-crystal silicon the reaction kinetics of nucleation and segregation of oxygen are already well established facts (4), as is the role of the oxygen in the thermal generation and locking of dislocations. Similarly well known is the nature of complexes between dislocation and oxygen precipitates.

In the case of polycrystalline silicon, on the other hand, it is only ascertained that oxygen segregates at GB in the 600°-900° range (5-9), while sensibly affecting the minority carrier lifetime (9), as in the case of oxygen precipitates in single-crystal silicon (10).

Furthermore, while in single-crystal silicon the beneficial effects of oxygen on impurity gettering are well established, the role of oxygen in homogeneous or heterogeneous reactions involving impurities in polycrystalline silicon is not yet clearly understood, as well as the role of oxygen in the electrical activation or deactivation of impurity centers.

Earlier results of Pizzini (11), Salama (12), and more recently of Zehaf (13), Martinuzzi (14), and Pizzini (15), could not be properly explained without assuming preferential interaction of metallic impurities with oxygen segregated at GB. This assumption, however, fails to provide any explanation for the synergistic effects of carbon.

The lifetime enhancement, which could be obtained by structural defect reduction consequent to a proper choice of the postgrowth annealing conditions (16), fits well in this frame; but still, the influence of other parameters, like the grain misorientation and the specific configuration of each GB on the segregation of oxygen, carbon (5, 6, 17), and impurities (18) during thermal annealing cycles and on the electrical properties of silicon, deserves further experimental attention.

Although a possible role of nitrogen on GB passivation was already proposed (19) by considering certain peculiar properties of polycrystalline silicon grown in Si_3N_4 crucibles (20) or treated with Si_3N_4 (21), it still needs fur-

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